ABSTRACT OF THE DISCLOSURE

An integrated circuit comprises a microprocessor for generating data signals along a data bus by way of an inverter to a plurality of input/output switching buffers. The buffers pass the data signals to a transmission bus for onward transmission to a receiving integrated circuit. A respective drain and source supply power to the buffers. A transition checking circuit monitors the number of data signals on the data bus simultaneously switching from a first to a second logic state and a control circuit counts the number of the simultaneous switching data signals and generates a flag signal when the count exceeds half the number of buffers. The flag signal is applied to the inverter to invert all of the data signals on the bus.